WEST Search History

| Hide Items | Restore | Clear | Cancel |

DATE: Friday, September 16, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT; PLUR=YES; OP=OR	
☐	L32	L30 and L16	9
☐	L31	L30 and L2	6
☐	L30	(conver$ near2 clock)	9386
☐	L29	(conver$ near2 clock) same (asic and (reprogrammable or programmable or pld or fpga))	7
☐	L28	conver$ near2 (clock$ near2 chain?)	3
☐	L27	L24 and simulat$	3723
☐	L26	L24 and L2	30
☐	L25	L24 and L16	58
☐	L24	edge near2 detect$	33192
☐	L23	L2 and (skew and race)	19
☐	L22	L21 and L16	52
☐	L21	L2 and synchronous	155
☐	L20	"synchronous primitive?"	11
☐	L19	L18 and L16	32
☐	L18	"clock source?"	8520
☐	L17	L16 and L3	139
☐	L16	"hardware accelerator"	1070
☐	L15	L13 and (verif$ or simulat$ or emulat$)	32
☐	L14	L13 and (verif$ or simulat$)	27
☐	L13	(conver$ near2 asic) near2 (fpga or pld)	45
☐	L12	(conver$ near2 asic) near2 programmable	1
☐	L11	(conver$ near2 asic) near2 reprogrammable	1
☐	L10	conver$ near2 asic	508
☐	L9	L4 and (large near2 asic)	7
☐	L8	L7 not L6	71
☐	L7	L4 and ((large near2 asic) or vlsi)	83
☐	L6	L5 and L3	29
☐	L5	accelerat$ near2 verification	94
☐	L4	L3 and L2	246

	L3	716/$[ccls] or 703/$[ccls]	15724
	L2	accelerat$ near2 simulat$	1271
	L1	hyduke[in] and stanley[in]	9

END OF SEARCH HISTORY

WEST Search History

DATE: Friday, September 16, 2005

Hide?	Set Name	Query	Hit Count
		DB=PGPB; PLUR=YES; OP=OR	
☐	L48	(insert$ near10 (edge near5 detect$))[clm]	17
☐	L47	("clock source?" and "synchronous primitive?")[clm]	1
☐	L46	(edge near5 detect$)[clm]	2434
☐	L45	(insert$ near5 "edge detector")[clm]	1
☐	L44	(find$ near5 "synchronous primitive?")[clm]	1
☐	L43	(find$ near5 "clock source?")[clm]	1
☐	L41	L40 and simulat$[clm]	4
☐	L40	"hardware accelerator"[clm]	60
☐	L39	(verification near2 manager)[clm]	11
☐	L38	(eliminat$ near3 "race conditions")[clm]	3
☐	L37	(eliminat$ near3 "clock skew")[clm]	2
☐	L36	(accelerat$ near3 verification)[clm]	7

END OF SEARCH HISTORY